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Remarks/Arguments:

Applicant's Attorney thanks the Examiner for the telephone interview on August 5, 2003. As discussed during the interview, the specification has been amended to more clearly indicate that Figs. 2-5 represent the problem addressed by the subject invention and not functioning prior art devices. In addition, the specification has been amended to more clearly indicate that a "block" of thyristors as used in the subject application means a block of contiguous thyristors. Finally, Applicants provide herewith a printout from the Delphion database indicating that Japanese patent no. 2807910 is the same as published Japanese patent application no. 3194978, which was submitted in the Information Disclosure Statement dated December 4, 2001.

Claims 5-7 and 9-12 are allowed in the subject application. Claims 1-4 and 8 are rejected under 35 U.S.C § 103(a) as being unpatentable over Applicant's prior art figures 1-5 and respective passages in the specification discussing said figures.

These rejections are based on a misunderstanding of Figures 1-5. Of these Figures, only Figure 1 represents a prior art device. This Figure is a schematic diagram from issued Japanese patent no. JP2807910B2 which is the same as published Japanese patent application JP3194978A2, as indicated on the print-out from the Delphion database transmitted herewith. The remaining figures 2-5 were not intended to illustrate prior art devices but to show the problem addressed by the subject invention. The specification has been amended to more clearly indicate that these Figures represent the problem and not functioning prior art devices.

Basis for the amendments to the paragraphs addressing Figs. 3-5 may be found at page 3, lines 5-9 which indicates that these Figures illustrate the problem addressed by the subject invention. Basis for the amendment to the paragraph addressing Fig. 2 may be found at page 2, lines 19-22 which describes the problem of intersecting lines. Basis for the amendment stating that the blocks B1, B2 and B3 include two contiguous transistors may be found in drawing Figs. 3, 4, 5, 7, 8, 11 and 12. No new matter is added by these amendments.

The Examiner states that claims 1 and 2 are not allowable over figure 2, which "shows a cross point (labeled 'cross') where a two-layer wiring is not shorted. (If there were a short, the

device would not be functional)." The Examiner further rejects claims 3-4 and 8 over features observable in one of figures 2 and 3.

Applicants respectfully disagree with the Examiner's analysis of figures 1-5. The Office Action assumes, since the devices illustrated in figures 1-5 are labeled "prior art", that the devices must be functional thyristor wiring schemes, wherein the labeled cross points are not actual shorts in the circuit. Figure 1 is incorporated from Fig. 3 of JP3194978 (the '978 application) which was cited in the Information Disclosure Statement dated December 4, 2001, and is merely a schematic showing device elements and connectivity between elements. The cross points in the '978 application were eliminated by the physical circuit layout shown in figures 4 and 8 of the '978 application. In those figures, parallel integrated circuits 101 provide the necessary signals to the gate electrodes G1 and G2, as well as anode electrodes A1-A8. Each gate electrode, G1 and G2, may then utilize cross-under wiring in order to connect to its respective thyristors, designated by anodes A1, A3, A5, A7 for G1 and A2, A4, A6, A8 for G2. Furthermore, two gate electrodes G1 and G2 are inherently required in the '978 invention, since the solution to cross points therein is to place an alternating array of anodes and thyristors on opposite sides of the device, alternately connected to one of gate electrodes G1 and G2.

The method used to eliminate the cross points of Fig. 3 in the '978 application, however, introduces undesirable additions to the device by requiring parallel ICs 101 to drive the electrodes. Further, as can be seen in Fig. 4 of the '978 application, and as described above, each thyristor gate in the illustrated device is not "separately connected to n gate-selecting lines", as in claims 1, 3, 5, and 8-9 of the subject application, nor are the "gates of n light-emitting thyristors included in each block commonly connected to one terminal" as in claims 2, 4, and 10.

Furthermore, it would be difficult if not impossible to modify the structure shown in Fig. 4 of the '978 application to connect "the gates of n light-emitting thyristors included in each block ... to one terminal" would require a wiring to extend beneath one of the thyristors as the two gate terminals are on opposite sides of the row of thyristors. The '978 application does not disclose or suggest how this would be done.

As for the "prior art" Figures 2-5 of the subject application, these Figures have been amended to delete the legend "Prior Art." Figure 2 of the subject application presents a

perspective view of a rearranged configuration the schematic drawing in Figure 1 so as to better illustrate the problem of cross points inherent in a device if it were manufactured according to the schematic drawing in Figure 1. Figures 3-5 show possible circuit layouts that may be desirable, but are described as being not feasible due to the shorts introduced by cross points as indicated. (See page 3, lines 5-9). Furthermore, it is noted that these drawing figures were not labeled "prior art" by Applicant. Instead, they were required to be labeled as such in the Office Action dated December 18, 2002. Because these Figures represent the problem and not the solution, Applicant acquiesced in labeling them as "Prior Art." This labeling, however, was not intended as an admission that any of these figures represents a functioning prior art device. Consequently, to avoid confusion, the "Prior Art" legends on Figures 2-5 are removed by this amendment. With these amendments it should be clear that none of the devices illustrated in Figures 2-5 represent functioning devices of the prior art. They are merely schematic drawings that have been presented to illustrate the problem of cross points and short circuits that would be introduced if the device were manufactured in a circuit layout according to those figures.

Thus, Applicants have established (in the subject application and in the cited prior art) that the devices shown in Figures 1 and 2 may be implemented less efficiently using techniques different from the inventive techniques and that the devices shown in Figures 3-5 are described as being not functional due to shorts introduced at the cross points indicated on these figures. Thus, the present invention, which, is aimed at eliminating the indicated cross points by claiming novel arrangements of thyristor matrix arrays, wherein cross points are eliminated in a way dissimilar to that taught in JP3194978, as discussed above can not be obvious in view of Applicant's admitted prior art. Thus, Claims 1-4 and 8 are not directed to the prior art figures 1-5, and thus are not subject to rejection under 35 U.S.C § 103(a) as being unpatentable over Applicant's admitted prior art figures 1-5.

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In view of the foregoing remarks, Applicant requests that the Examiner reconsider and withdraw the final rejection of claims 1-4 and 8.

Respectfully submitted,

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Dated: August 6, 2003

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August 6, 2003

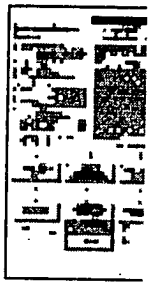
Tonya M. Berger

The Delphion Integrated View

Title: **JP3194978A2: LIGHT EMITTING ELEMENT ARRAY**

Country: **JP** Japan
Kind: **A**

Inventor: **KUSUDA YUKIHISA;**



Assignee: **NIPPON SHEET GLASS CO LTD**
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Published / Filed: **1991-08-26** / 1989-12-22

Application Number: **JP1989000334485**

IPC Code: **H01L 33/00;** B41J 2/44; B41J 2/45; B41J 2/455; G03G 15/04;

Priority Number: 1989-12-22 **JP1989000334485**

Abstract:

PURPOSE: To reduce the necessary number of electrodes, to enhance resolution, to reduce its cost and to raise reliability by providing a light emitting element block including a plurality of light emitting elements, a plurality of first electrodes for supplying first signals, and a plurality of second electrodes for supplying second signals.

CONSTITUTION: Light emitting element blocks B including a plurality of light emitting elements T for emitting lights when first and second signals are simultaneously supplied, a plurality of electrodes A for supplying the first signals to the elements T in the block B to be provided in the blocks B, and a plurality of second electrodes G for supplying the second signals to the elements T to be provided at the elements T corresponding to the blocks B are provided. Thus, the number of electrodes can be reduced, and since the arraying pitch of the elements can be reduced, its resolution can be enhanced, its cost can be reduced, and high reliability is performed.

INPADOC Legal Status: None **Get Now:** Family Legal Status Report

Family:

PDF	Publication	Pub. Date	Filed	Title
	JP3194978A2	1991-08-26	1989-12-22	LIGHT EMITTING ELEMENT ARRAY
☑	JP2807910B2	1998-10-08	1989-12-22	HATSUKOSOSHIAREI
2 family members shown above				

Forward References:

PDF	Patent	Pub.Date	Inventor	Assignee	Title
	US6563526	2003-05-13	Sekiya; Toshiyuki	Canon Kabushiki Kaisha	Image formation apparatus
	US6498356	2002-12-24	Sekiya; Toshiyuki	Canon Kabushiki Kaisha	LED chip, LED array chip, LE head and image-forming app
	US6461883	2002-10-08	Mine; Ryuta	Canon Kabushiki Kaisha	Method for manufacturing lec head and led array head prep using the same
	US6442361	2002-08-27	Shiraishi; Mitsuo	Canon Kabushiki Kaisha	Variable speed image format apparatus and method
	US6392615	2002-05-21	Shiraishi; Mitsuo	Canon Kabushiki Kaisha	Drive apparatus and method emission element array
	US6323887	2001-11-27	Shiraishi; Mitsuo	Canon Kabushiki Kaisha	Color image forming apparat driving a recording-element a a method for controlling the s

Other Abstract Info: DERABS G91-292198 DERG91-292198

Date: August 6, 2003

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NAME Shunsuke Ohtsuka et al.

DOCUMENTS Transmittal; Amendment After Final (7pgs); Amended Drwgs. (4 sheets); Printout from Delphion database (2pgs); Postcard

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